IN THE CLAIMS:

The following listing of claims will replace all prior versions, and listings, of claims in the application.

1 – 41. (Cancelled)

42. (Currently Amended) A method for delaying output of a digital marker signal with respect to output of a data signal in an arbitrary waveform generator, the method comprising:

determining a relative delay between the digital marker signal and the data signal based upon a travel path of the digital marker signal and a travel path of the data signal, wherein the data signal is a waveform output by the arbitrary waveform generator and wherein the digital marker signal indicates a predetermined position in the waveform; and

programming a marker delay circuit to delay the output of the digital marker signal to output the digital marker signal at [[a]] the predetermined position with respect to the output of the data signal, based on the determined relative delay.

43. (Original) The method of claim 42, wherein said programming a marker delay circuit to delay the output of the digital marker signal to output the digital marker signal at a predetermined position with respect to the output of the data signal, based on the determined relative delay, comprises automatically programming the marker delay circuit to add the relative delay to the output of the digital marker signal to automatically align the output of the digital marker signal in time with respect to the output of the data signal.

44. (Cancelled)

45. (Original) The method of claim 42, wherein said determining a relative delay between the digital marker signal and the data signal based upon a travel path of the digital marker signal and a travel path of the data signal comprises automatically determining a total path delay associated with the data signal.

46. (Original) The method of claim 45, wherein said determining a relative delay between the digital marker signal and the data signal based upon a travel path of the digital marker signal and a travel path of the data signal further comprises automatically determining a total path delay associated with the digital marker signal.

47. (Original) The method of claim 46, wherein said determining a relative delay between the digital marker signal and the data signal based upon a travel path of the digital marker signal and a travel path of the data signal further comprises automatically determining the relative delay by calculating the difference between the total path delay associated with the data signal and the total path delay associated with the digital marker signal.

48. (Original) The method of claim 45, wherein said automatically determining the total path delay associated with the data signal comprises determining a variable path delay associated with the travel path of the data signal.

49. (Original) The method of claim 48, wherein said automatically determining the total path delay associated with the data signal further comprises determining a fixed path delay associated with the travel path of the data signal.

50. (Original) The method of claim 49, wherein said automatically determining the total path delay associated with the data signal further comprises calculating the total path delay associated with the data signal using the fixed path delay and the variable path delay.

51. (Original) The method of claim 46, wherein said automatically determining the total path delay associated with the digital marker signal comprises detecting a fixed path delay and a variable path delay associated with the travel path of the digital marker signal.

52. (Original) The method of claim 42, wherein said programming a marker delay circuit to delay the output of the digital marker signal to output the digital marker signal at a predetermined position with respect to the output of the data signal, based on the determined relative delay, comprises receiving a user input indicating an additional delay to program the marker delay circuit to add the determined relative delay plus the additional delay to the output of the digital marker signal to output the digital marker signal at the predetermined position in time with respect to the output of the data signal.

53. (Original) The method of claim 42, wherein said programming a marker delay circuit to delay the output of the digital marker signal to output the digital marker signal at a predetermined position with respect to the output of the data signal, based on the determined relative delay, comprises receiving a user input reducing the determined relative delay to program the marker delay circuit to add the reduced relative delay to the output of the digital marker signal to output the digital marker signal at the predetermined position in time with respect to the output of the data signal.

54. (Original) The method of claim 42, wherein said programming a marker delay circuit to delay the output of the digital marker signal to output the digital marker signal at a predetermined position with respect to the output of the data signal, based on the determined relative delay, comprises receiving a user input to program the marker delay circuit to add a desired delay to the output of the digital marker signal to output the digital marker signal at the predetermined position in time with respect to the output of the data signal.

55. (Original) The method of claim 42, wherein the data signal is output in analog form.

56. (Original) The method of claim 42, where in the data signal is output in digital form.

57. (Original) The method of claim 42, further comprising:

sensing a temperature associated with one or more delay elements associated with at least one of the travel paths of the digital marker signal and the data signal to adjust the relative delay based on the sensed temperature.

58. (Original) The method of claim 42, further comprising:

asserting a status notification bit associated with the digital marker signal to notify a user about an occurrence of the digital marker signal.

59. (Original) The method of claim 58, further comprising:

programming a status notification delay circuit to delay assertion of the status notification bit.

60. (Original) The method of claim 42, wherein the relative delay between the digital marker signal and the data signal is dependent upon at least one or more of:

delays associated with one or more analog filters;

delays associated with one or more amplifiers;

delays associated with signal paths;

delays associated with sampling rates;

delays associated with interpolation rates of one or more DACs;

delays associated with output terminals; and

delays associated with one or more FFGAs.

61. (Currently Amended) ~~An apparatus~~ A waveform generator, comprising:

first circuitry for generating a data signal as an output of the waveform generator;

second circuitry for generating a digital marker signal, wherein the digital marker signal indicates a predetermined position with respect to the output of the data signal;

a delay determining unit operable to determine a relative delay between [[a]] the digital marker signal and the data signal based upon a travel path of the digital marker signal and a travel path of the data signal; and

a marker delay circuit configured to be programmed to delay output of the digital marker signal to output the digital marker signal at a predetermined position with respect to the output of the data signal, based on the determined relative delay.

62. (Original) The apparatus of claim 61, wherein the marker delay circuit is configured to be automatically programmed to add the relative delay to the output of the digital marker signal to automatically align the output of the digital marker signal in time with respect to the output of the data signal.

63. (Cancelled)

64. (Original) The apparatus of claim 61, wherein the delay determining unit is operable to automatically determine a total path delay associated with the data signal.

65. (Original) The apparatus of claim 64, wherein the delay determining unit is also operable to automatically determine a total path delay associated with the digital marker signal.

66. (Original) The apparatus of claim 65, wherein the delay determining unit is also operable to automatically determining the relative delay by calculating the difference between the total path delay associated with the data signal and the total path delay associated with the digital marker signal.

67. (Original) The apparatus of claim 64, wherein said automatically determining the total path delay associated with the data signal comprises the delay determining unit determining a variable path delay associated with the travel path of the data signal.

68. (Original) The apparatus of claim 67, wherein said automatically determining the total path delay associated with the data signal further comprises the delay determining unit determining a fixed path delay associated with the travel path of the data signal.

69. (Original) The apparatus of claim 68, wherein said automatically determining the total path delay associated with the data signal further comprises the delay determining unit calculating the total path delay associated with the data signal using the determined fixed path delay and the determined variable path delay.

70. (Original) The apparatus of claim 65, wherein said automatically determining the total path delay associated with the digital marker signal comprises the delay determining unit detecting a fixed path delay and a variable path delay associated with the travel path of the digital marker signal.

71. (Original) The apparatus of claim 61, wherein the delay determining unit is operable to receive a user input indicating an additional delay and to program the marker delay circuit to add the determined relative delay plus the additional delay to the output of the digital marker signal to output the digital marker signal at the predetermined position in time with respect to the output of the data signal.

72. (Original) The apparatus of claim 61, wherein the delay determining unit is operable to receive a user input reducing the determined relative delay and to program the marker delay circuit to add the reduced relative delay to the output of the digital marker signal to output the digital marker signal at the predetermined position in time with respect to the output of the data signal.

73. (Original) The apparatus of claim 61, wherein the travel path of the data signal is separate from the travel path of the digital marker signal.

74. (Original) A method for delaying output of a first data signal provided by a first waveform generator with respect to output of a second data signal provided by a second waveform generator, the method comprising:

determining a relative delay between the first data signal provided by the first waveform generator and the second data signal provided by the second waveform

generator, based upon a travel path of the first data signal and a travel path of the second data signal; and

programming a data pipeline delay circuit, based on the determined relative delay, to delay the output of the first data signal to output the first data signal at a predetermined position with respect to the output of the second data signal.

75. (Original) The method of claim 74, wherein said programming a data pipeline delay circuit, based on the determined relative delay, to delay the output of the first data signal to output the first data signal at a predetermined position with respect to the output of the second data signal comprises automatically programming the data pipeline delay circuit to add the relative delay to the output of the first data signal to automatically align the output of the first data signal with respect to the output of the second data signal.

76. (Original) The method of claim 74, wherein said determining a relative delay between the first data signal provided by the first waveform generator and the second data signal provided by the second waveform generator, based upon a travel path of the first data signal and a travel path of the second data signal, comprises automatically determining a total path delay associated with the first data signal provided by the first waveform generator.

77. (Original) The method of claim 76, wherein said determining a relative delay between the first data signal provided by the first waveform generator and the second data signal provided by the second waveform generator, based upon a travel path of the first data signal and a travel path of the second data signal, further comprises automatically determining a total path delay associated with the second data signal provided by the second waveform generator.

78. (Original) The method of claim 77, wherein said determining a relative delay between the first data signal provided by the first waveform generator and the second data signal provided by the second waveform generator, based upon a travel path of the first data signal and a travel path of the second data signal, further comprises

automatically determining the relative delay by calculating the difference between the total path delay associated with the first data signal and the total path delay associated with the second data signal.

79. (Original) The method of claim 76, wherein said automatically determining the total path delay associated with the first data signal comprises determining a variable path delay associated with the travel path of the first data signal.

80. (Original) The method of claim 79, wherein said automatically determining the total path delay associated with the first data signal further comprises determining a fixed path delay associated with the travel path of the first data signal.

81. (Original) The method of claim 80, wherein said automatically determining the total path delay associated with the first data signal further comprises calculating the total path delay associated with the first data signal using the determined fixed path delay and the determined variable path delay.

82. (Original) The method of claim 74, wherein the relative delay between the first data signal provided by the first waveform generator and the second data signal provided by the second waveform generator is dependent upon at least one or more of:

delays associated with one or more analog filters;
delays associated with one or more amplifiers;
delays associated with signal paths;
delays associated with sampling rates;
delays associated with interpolation rates of one or more DACs;
delays associated with output terminals; and
delays associated with one or more FFGAs.

83. (Original) The method of claim 74, wherein said programming a data pipeline delay circuit, based on the determined relative delay, to delay the output of the first data signal to output the first data signal at a predetermined position with respect to the output of the

second data signal comprises receiving a user input indicating an additional delay to program the data pipeline delay circuit to add the determined relative delay plus the additional delay to the output of the first data signal to output the first data signal at the predetermined position with respect to the output of the second data signal

84. (Original) The method of claim 74, wherein said programming a data pipeline delay circuit, based on the determined relative delay, to delay the output of the first data signal to output the first data signal at a predetermined position with respect to the output of the second data signal comprises receiving a user input reducing the determined relative delay to program the data pipeline delay circuit to add the reduced relative delay to the output of the first data signal to output the first data signal at a predetermined position with respect to the output of the second data signal.

85. (Original) The method of claim 74, wherein said programming a data pipeline delay circuit, based on the determined relative delay, to delay the output of the first data signal to output the first data signal at a predetermined position with respect to the output of the second data signal comprises receiving a user input to program the data pipeline delay circuit to add a desired delay to the output of the first data signal to output the first data signal at a predetermined position with respect to the output of the second data signal.

86. (Original) A system, comprising:

a first waveform generator;

a second waveform generator coupled to the first waveform generator;

a delay determining unit operable to determine a relative delay between the first data signal provided by the first waveform generator and the second data signal provided by the second waveform generator, based upon a travel path of the first data signal and a travel path of the second data signal; and

a data pipeline delay circuit to be programmed, based on the determined relative delay, to delay the output of the first data signal to output the first data signal at a predetermined position with respect to the output of the second data signal.

87. (Original) The system of claim 86, wherein the data pipeline delay circuit is configured to be automatically programmed to add the relative delay to the output of the first data signal to automatically align the output of the first data signal with respect to the output of the second data signal.

88. (Original) The system of claim 86, wherein the delay determining unit is also operable to automatically determine a total path delay associated with the first data signal provided by the first waveform generator.

89. (Original) The system of claim 88, wherein the delay determining unit is further operable to automatically determine a total path delay associated with the second data signal provided by the second waveform generator.

90. (Original) The system of claim 89, wherein the delay determining unit is further operable to automatically determine the relative delay by calculating the difference between the total path delay associated with the first data signal and the total path delay associated with the second data signal.

91. (Original) The system of claim 88, wherein automatically determine a total path delay associated with the first data signal provided by the first waveform generator comprises the delay determining unit determining a variable path delay associated with the travel path of the first data signal.

92. (Original) The system of claim 91, wherein automatically determine a total path delay associated with the first data signal provided by the first waveform generator further comprises the delay determining unit determining a fixed path delay associated with the travel path of the first data signal.

93. (Original) The system of claim 92, wherein automatically determine a total path delay associated with the first data signal provided by the first waveform generator further comprises the delay determining unit calculating the total path delay associated

with the first data signal using the determined fixed path delay and the determined variable path delay.

94. (Original) The system of claim 86, wherein the delay determining unit is operable to receive a user input indicating an additional delay to program the data pipeline delay circuit to add the determined relative delay plus the additional delay to the output of the first data signal to output the first data signal at the predetermined position with respect to the output of the second data signal.

95. (Original) The system of claim 86, wherein the delay determining unit is operable to receive a user input reducing the determined relative delay to program the data pipeline delay circuit to add the reduced relative delay to the output of the first data signal to output the first data signal at a predetermined position with respect to the output of the second data signal.